

- GPIO25\_USB3.0\_EN
- GPIO24\_USB3.0\_FAULT
- GPIO22\_USB2.0\_EN
- GPIO23\_USB2.0\_FAULT
- GPIO25\_USB3.0\_EN
- GPIO24\_USB3.0\_FAULT
- GPIO22\_USB2.0\_EN
- GPIO23\_USB2.0\_FAULT

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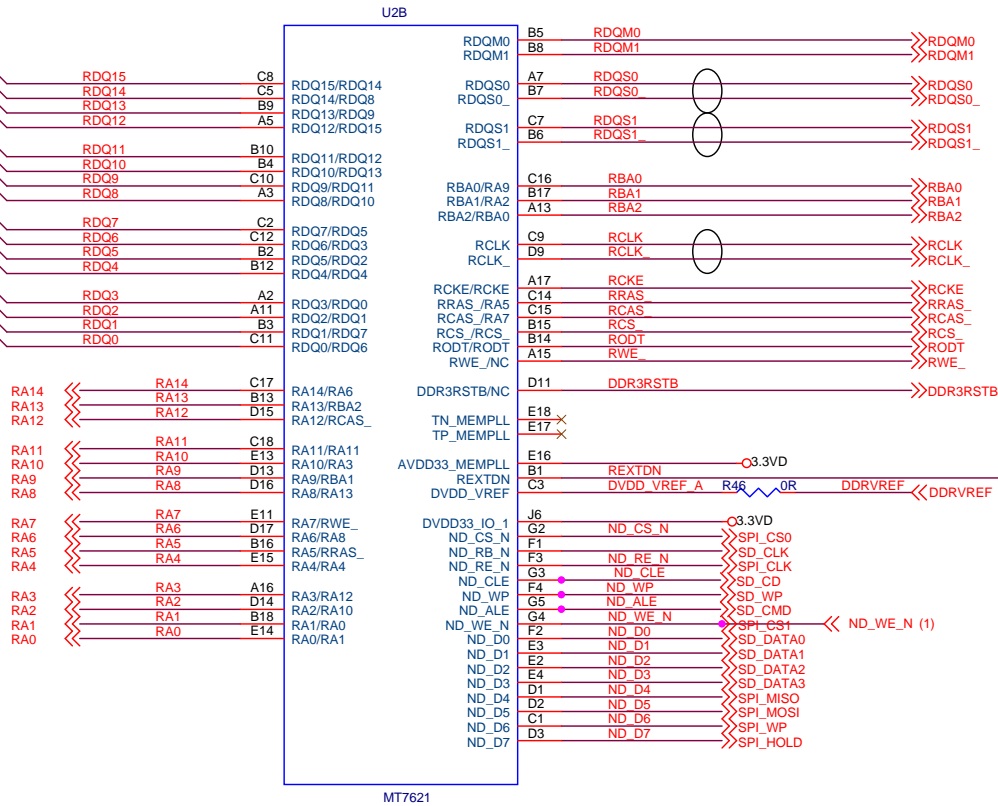
**MT7621A**

File	MT7621A	Drawn	Jimmy	Rev	V11
Size	Document Number MT7621A	Date	Tuesday, May 15, 2015	Sheet	2 of 15

RDQ[0:15]

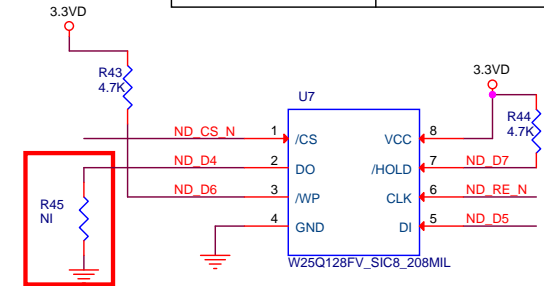
DDR3/DDR2 Interface  
The pinout is different when use DDR3 and DDR2

diff pair

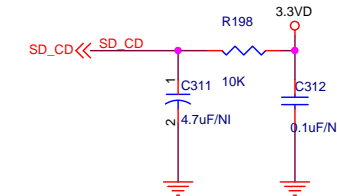
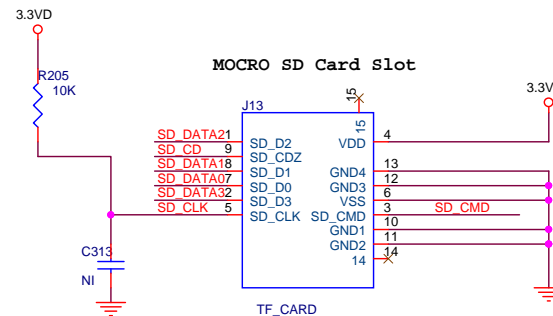
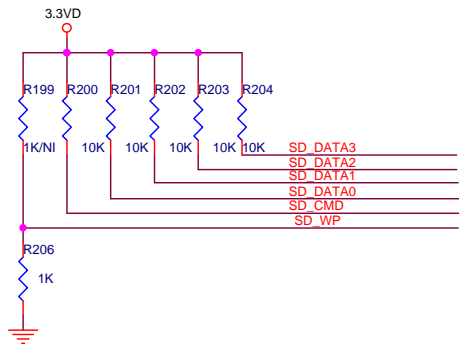
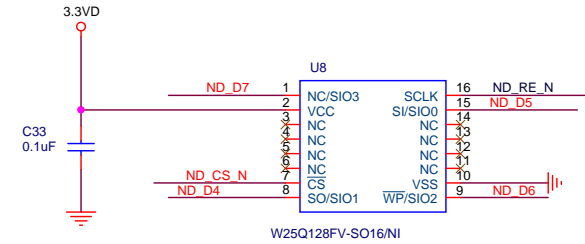


Test Pad for signal measurement

spi_cs0 (I/O)	nd_cs_n (0)
spi_cs1 (I/O)	nd_we_n (0)
spi_clk (I/O)	nd_re_n (0)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)



SPI Flash

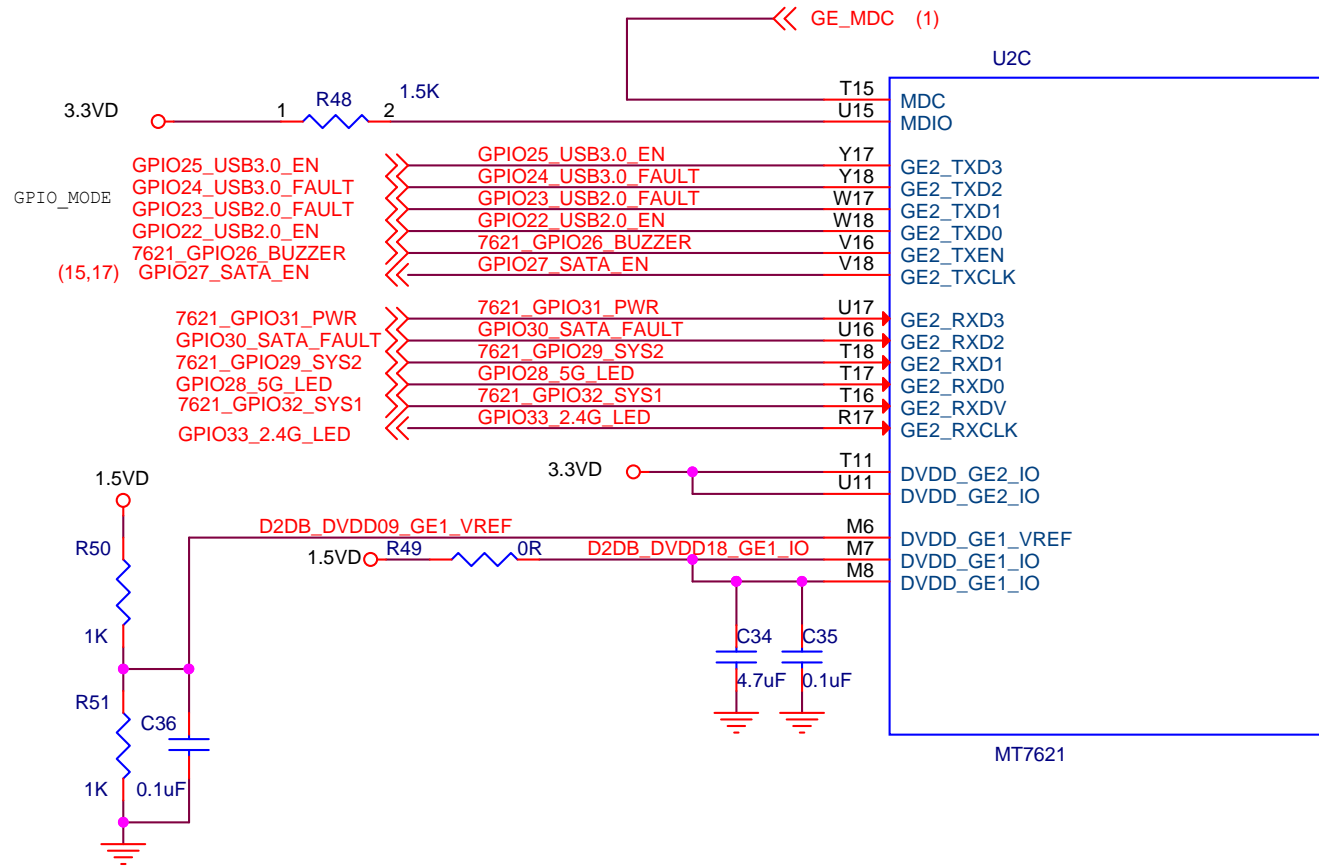


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Title		MT7621A	
Size	Document Number	Drawn	Rev
B	MT7621A	Jimmy	V11
Date:	Tuesday, May 19, 2015	Sheet	3 of 15

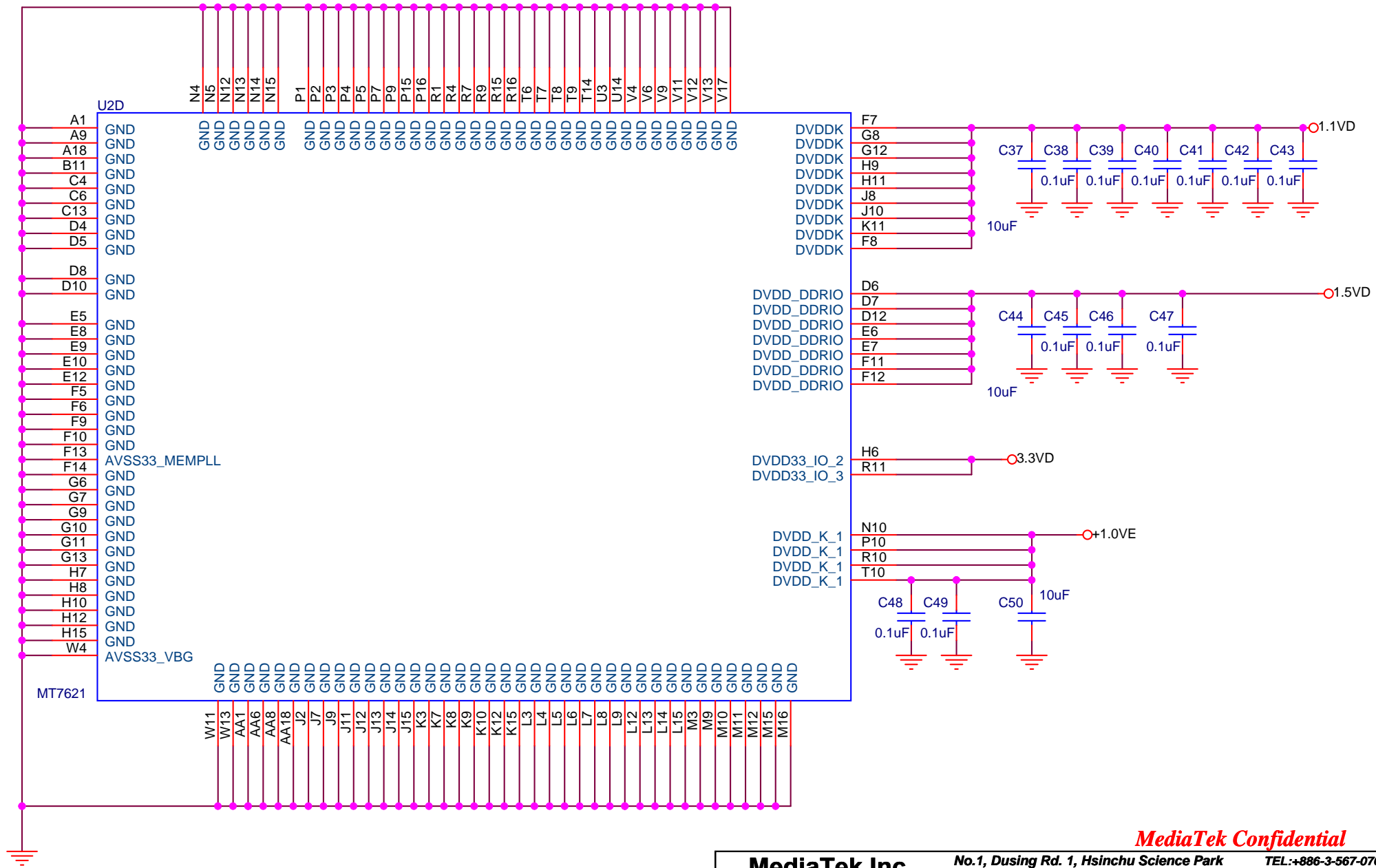
# RGMII Interface



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		<b>Title</b> <b>MT7621A</b>			
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Date: Tuesday, May 19, 2015		Sheet 4	of	15	

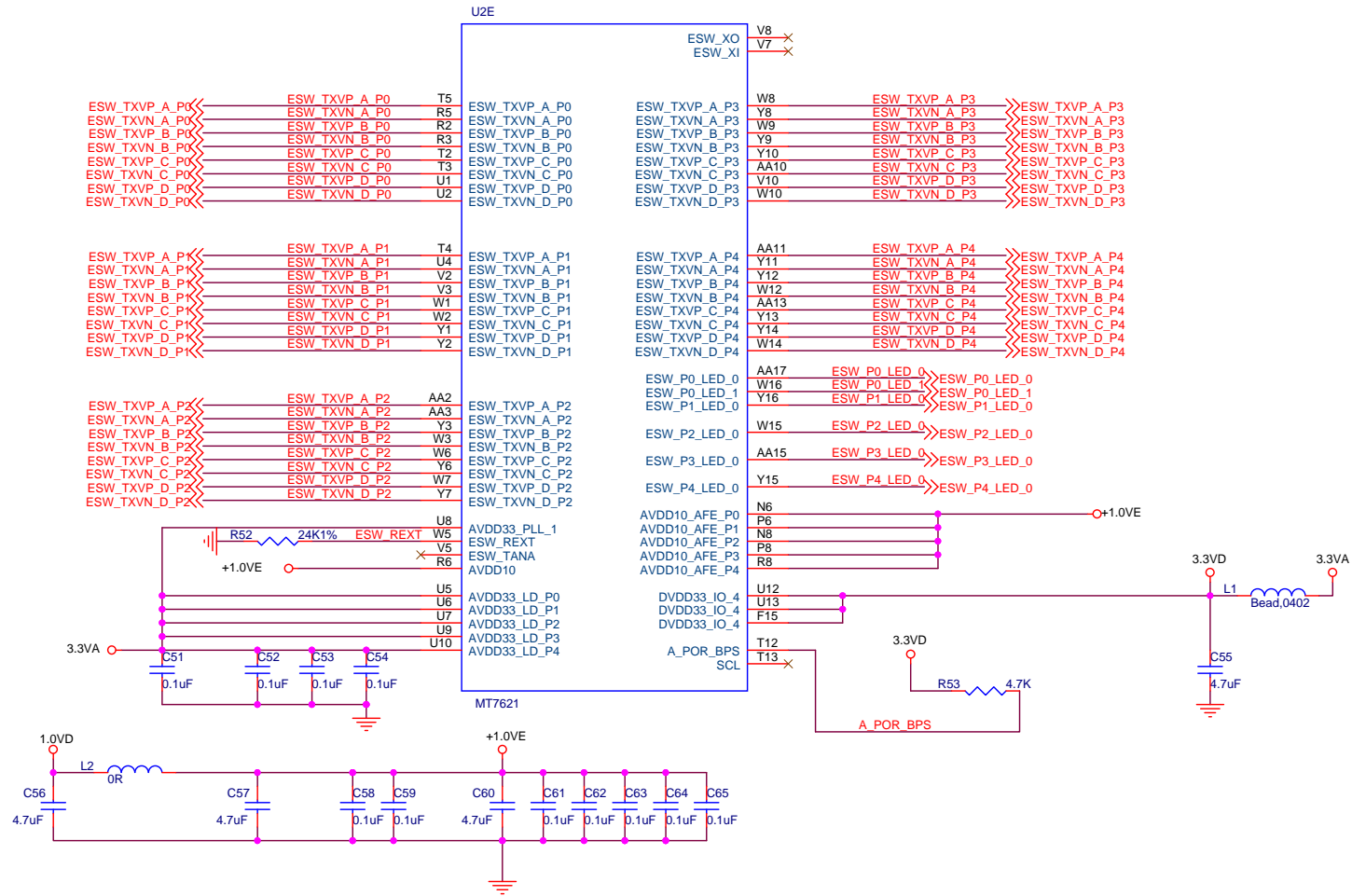
# MT7621 Power



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Date:	Tuesday, May 19, 2015			Sheet	5 of 15

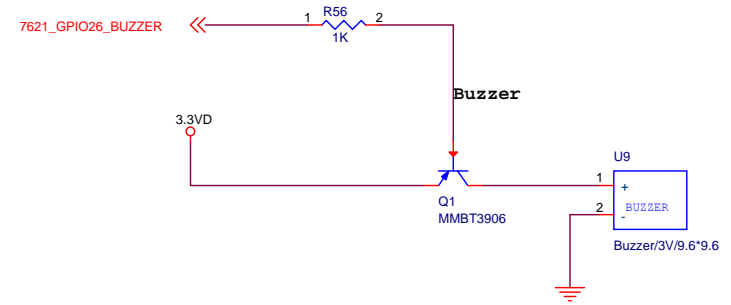
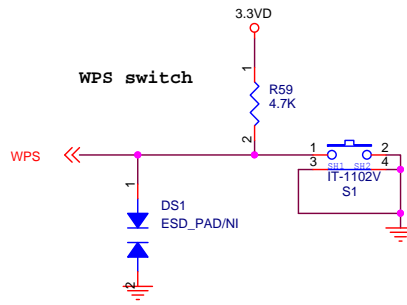
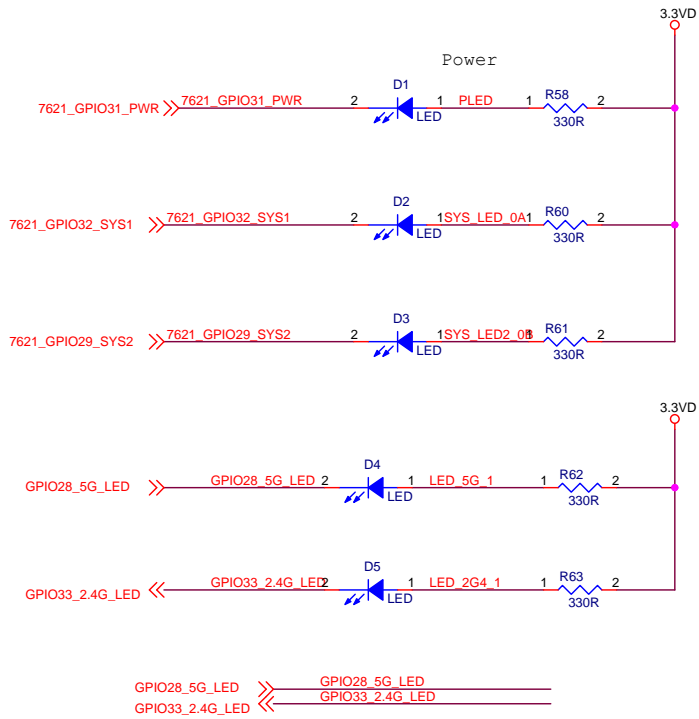
# Giga SW



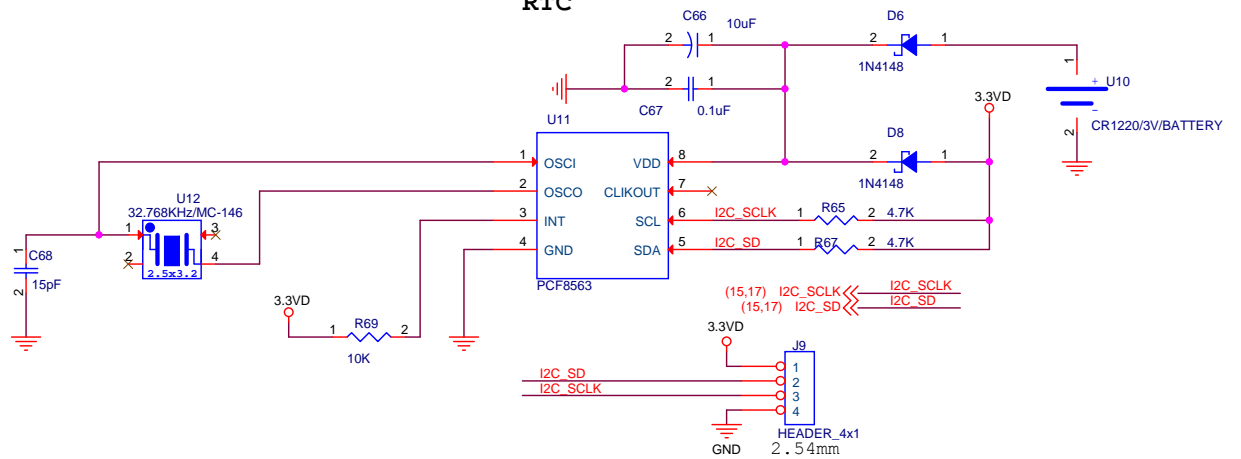
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Size	Document Number	Drawn	Rev	
B	MT7621A	Jimmy	V11	
Date:	Tuesday, May 19, 2015	Sheet	6	of 15

# LED

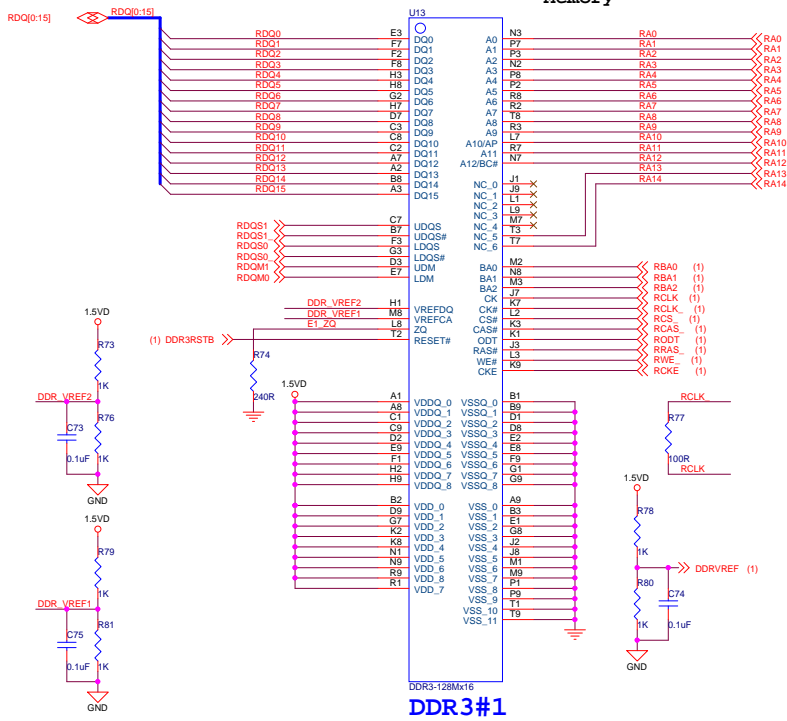


# RTC

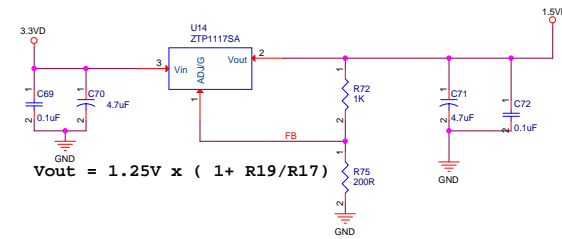


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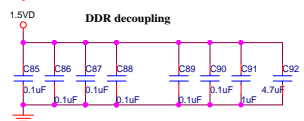
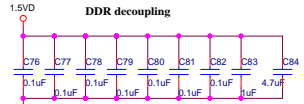
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Title		MT7621A		
Size	Document Number	Drawn	Rev	
B	MT7621A	Jimmy	V11	
Date:	Tuesday, May 19, 2015	Sheet	7	of 15



DDR3#1



$$V_{out} = 1.25V \times (1 + R19/R17)$$



4.7u\*2+0.6u

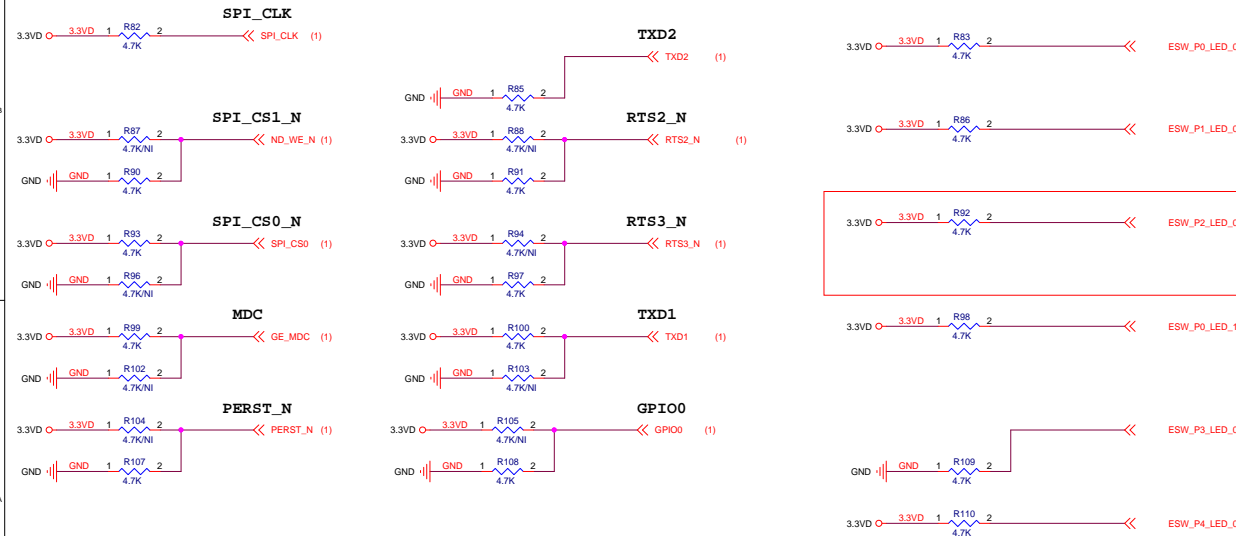


### Boot Strapping

Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM 1: DRAM configuration from Auto Detect	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input 011: 40 MHz, Self Oscillation mode 0101: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input	
PERST_N	OCP_RATIO	0: 1:3 1: 1:4	
TXD2	DRAM_TYPE	0: DDR3 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0 }	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) 0010: Normal / Boot from SPI 3-byte address 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

### Giga Switch Hardware Trap

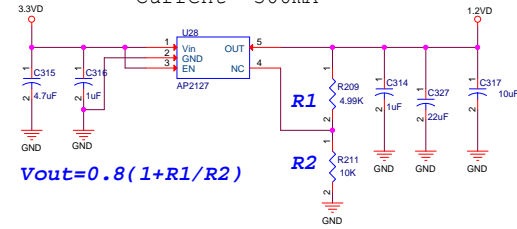
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] □ 4'b0000: IDDQ mode □ 4'b0001: IOTEST mode □ 4'b0010: NANDTREE mode □ 4'b0011: RING mode (both IO and std-cell) □ 4'b0100: MBIST □ 4'b0101: SCAN mode (internal) □ 4'b0110: SCAN-COMP mode (compression) □ 4'b0111: SCAN-MBIST-OLT mode □ 4'b1000: AFE-OLT mode □ 4'b1001: GPHY ATE mode □ 4'b1010: GPHY ADUMP mode □ 4'b1011: GPHY ADUMP probe mode □ 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection □ xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



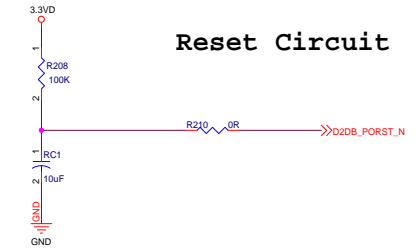
System Power

For USB/PCIe PHY Power (1.2V)

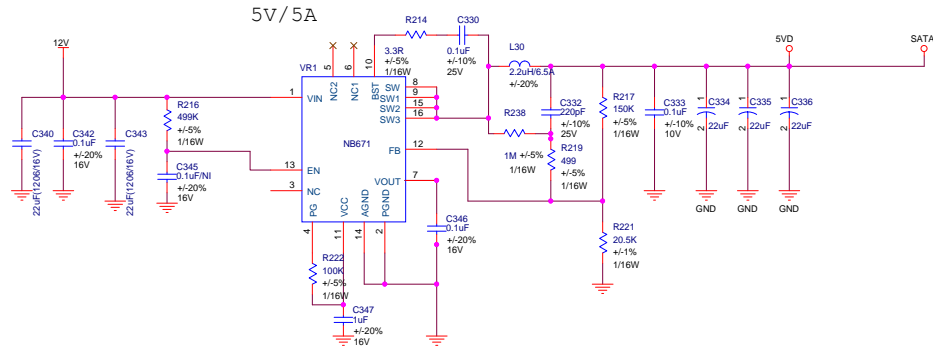
Current= 300mA



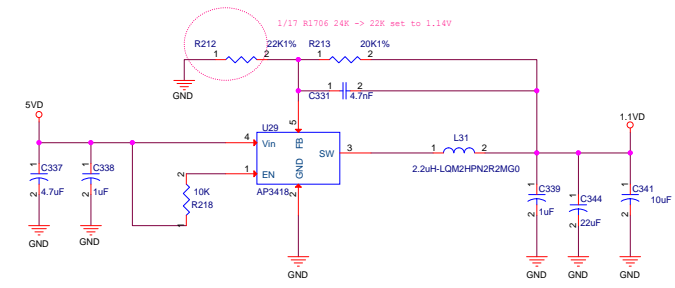
Reset Circuit



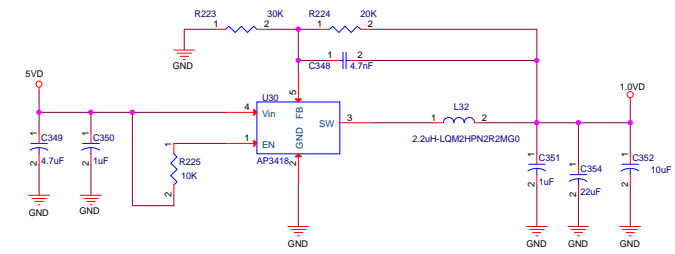
5V/5A



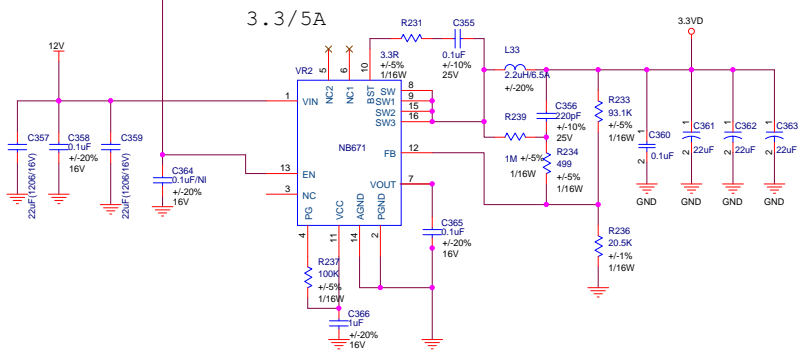
1.14V/1.5A



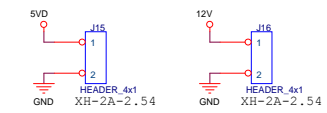
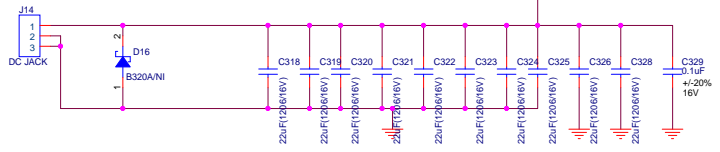
1.0V/1.5A

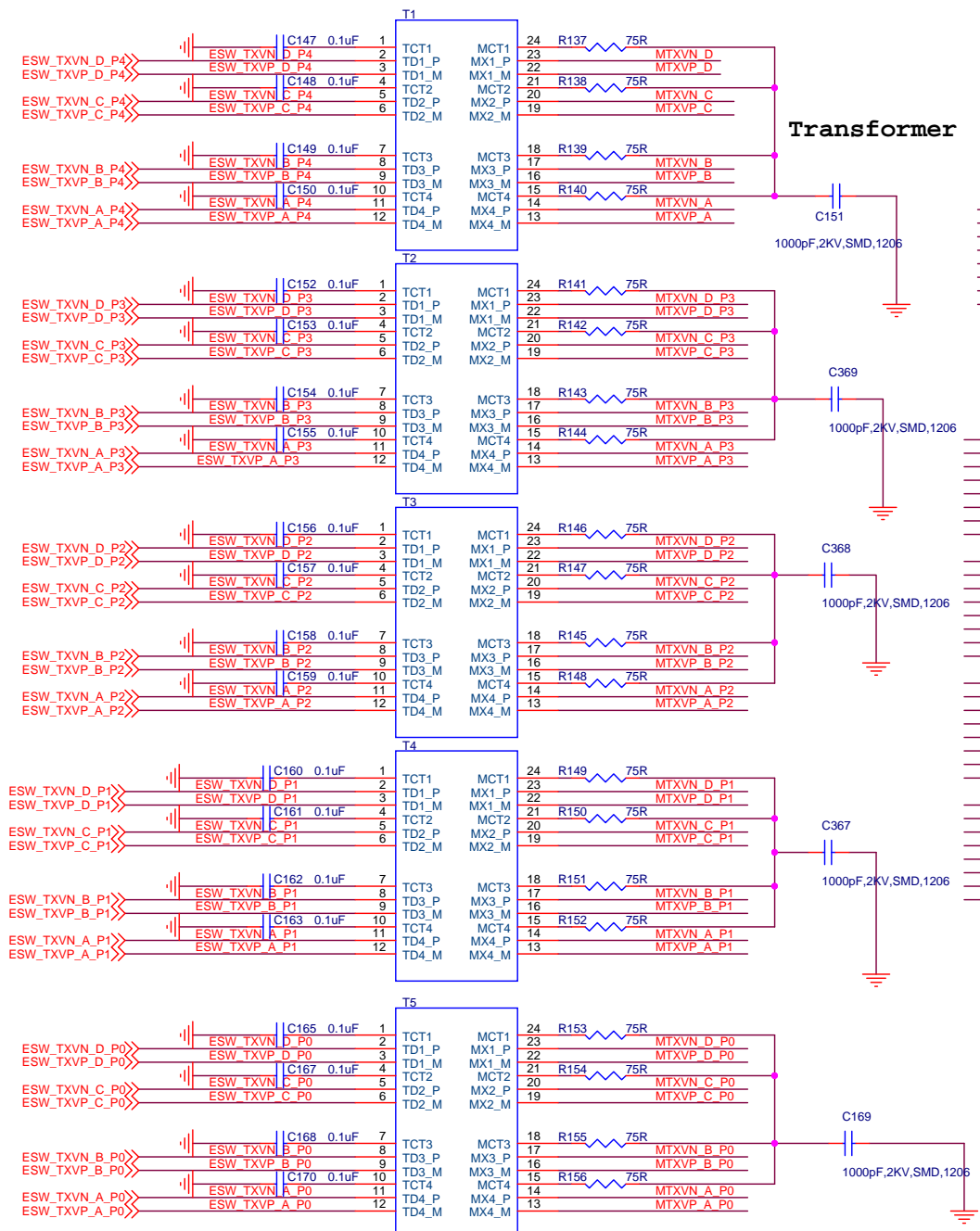


3.3/5A

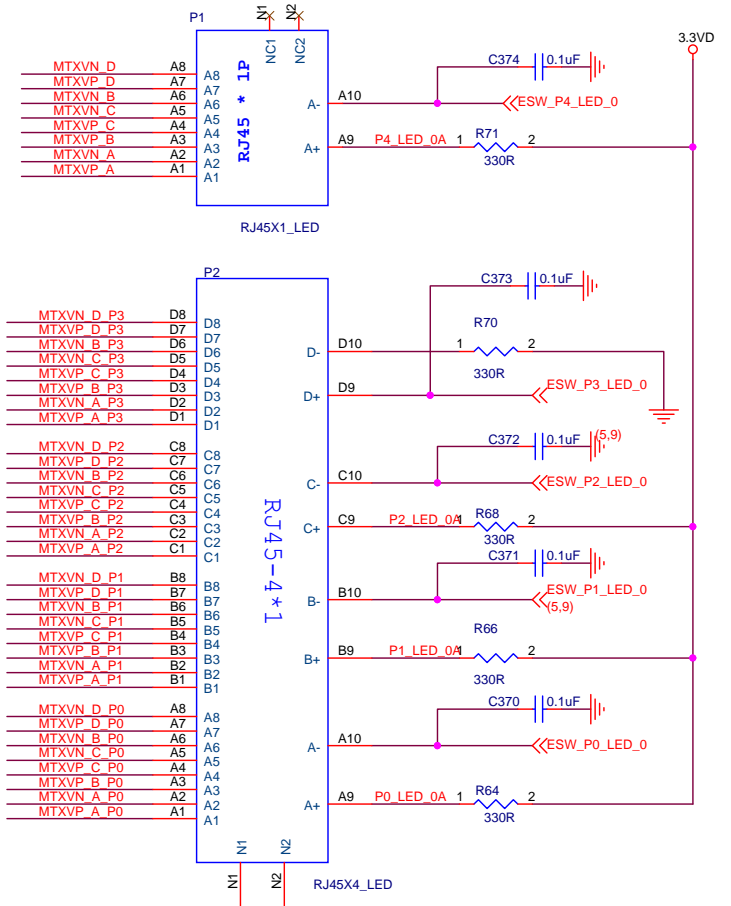


214110130000001  
3.8/1.3





**Transformer**

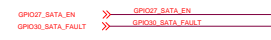
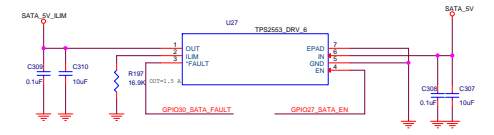
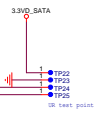
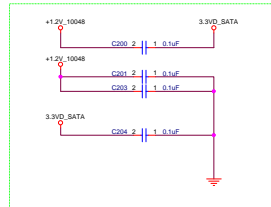
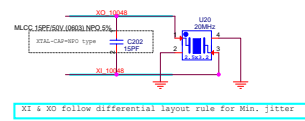
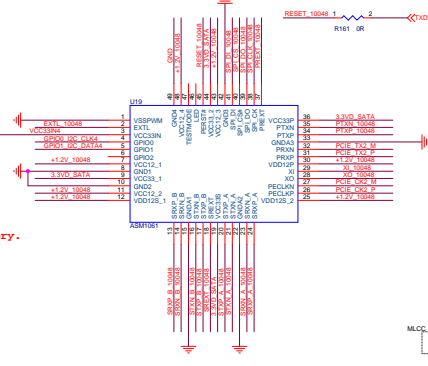
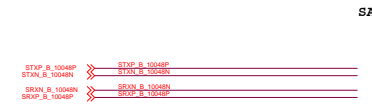
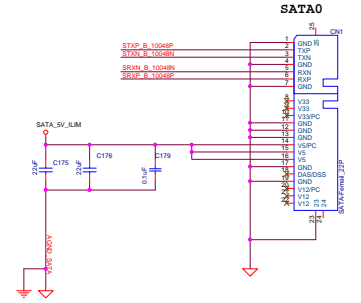
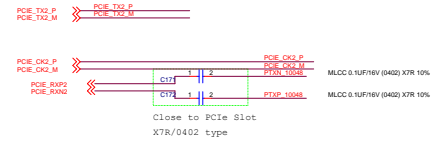
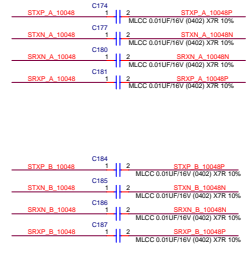
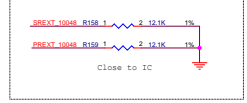
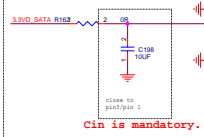
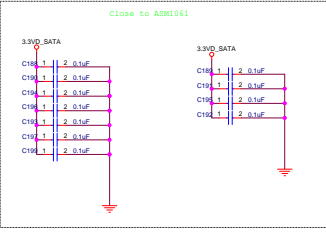
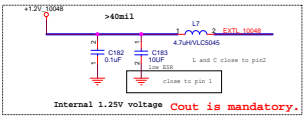
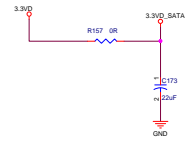
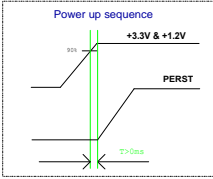


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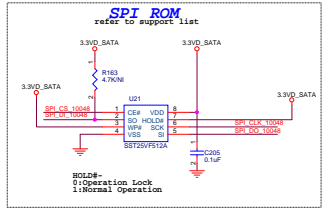
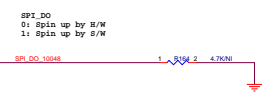
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Title		MT7621A	
Size	Document Number	Drawn	Rev
B	MT7621A	Jimmy	V11
Date:	Tuesday, May 19, 2015	Sheet	11 of 15

PCIe to SATA



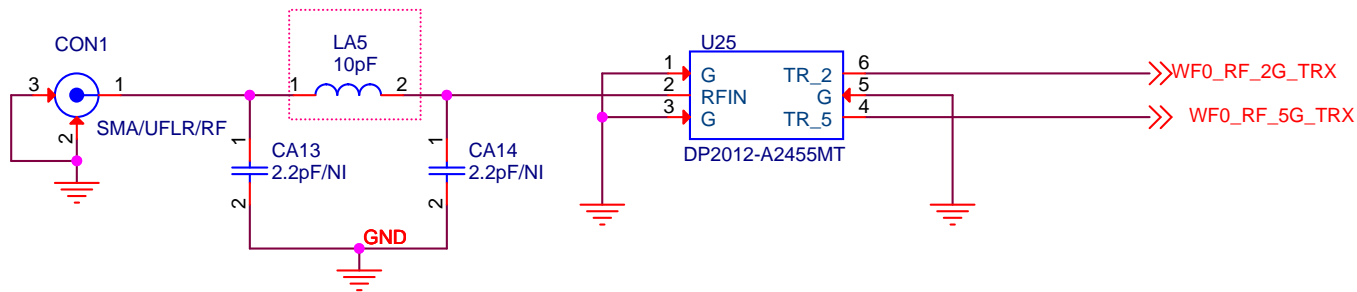
H/W Strapping



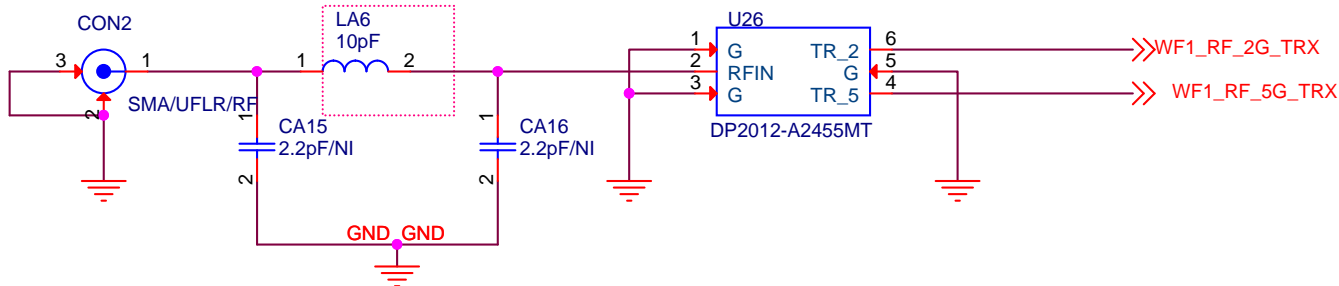




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Date:	Tuesday, May 19, 2015	Sheet 15 of 15